INTEGRATED CIRCUIT DEVICE INCLUDING A SCAN TEST CIRCUIT AND METHODS OF TESTING THE SAME

ABSTRACT OF THE DISCLOSURE

Integrated circuit devices include a core block having a plurality of output ports and a plurality of input ports and a vector input terminal. The core block generates core internal data responsive to output data from the input ports. The core block is configured to output the core internal data during scan testing and to selectively generate core output data for the output ports responsive to the core internal data or to test vector serial input data from the vector input terminal. An input side sub logic circuit unit is configured for dynamic simulation testing and is coupled to the input ports of the core block. The input side sub logic circuit unit generates sub data for the plurality of input ports responsive to data input to the first sub logic circuit unit. A multiplexer (MUX) unit between the core block and the first sub logic circuit unit selectively provides the sub data or the output data as inputs to the input ports of the core block responsive to a MUX control signal. Methods of testing the integrated circuit devices are also provided.

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